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Antonio Franques

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Education

2015–Present 
University of Illinois at Urbana-Champaign
Ph.D. Computer Science
Advisor: Professor Josep Torrellas
Area: Computer Architecture, Parallel Computing, Systems

2011–2015 
Polytechnic University of Valencia (UPV), Spain
B.S. Telecommunications Engineering, GPA: 8.9/10, Ranked 2nd in graduating class
Thesis: Numerical Methods for Nonlinear Modeling (Grade: 10/10)
Advisors: Professors Juan Ramón Torregrosa and Alicia Cordero
Overseas studies: Norwegian University of Science and Technology (NTNU), Fall 2014

Publications

May 2018 — X. Timoneda, S. Abadal, A. Cabellos-Aparicio, D. Manessis, J. Zhou, **A. Franques**, J. Torrellas, E. Alarcon, *"Millimeter-Wave Propagation within a Computer Chip Package"*, ISCAS '18.

Nov. 2017 — V. Fernando, **A. Franques**, S. Abadal, S. Misailovic, J. Torrellas, *"Adapting Programs for Wireless On-Chip Communication"*, submitted to ISCA '18.

May 2016 — A. Cordero, **A. Franques** and J.R. Torregrosa, *"Chaos and Convergence of a family generalizing Homeier's method with damping parameters"*, Nonlinear Dynamics, doi: 10.1007/s11071-016-2807-0.

June 2015 — A. Cordero, **A. Franques** and J.R. Torregrosa, *"Multidimensional Homeier's generalized class and its application to planar 1D Bratu problem"*, SeMA Journal, doi: 10.1007/s40324-015-0037.

May 2015 — A. Cordero, **A. Franques** and J.R. Torregrosa, *"Numerical solution of turbulence problems by solving Burgers' equation"*, Algorithms 8 (2015) 224-233, doi: 10.3390/a8020224.

Sept. 2014 — A. Cordero, L. Feng, **A. Franques** and J.R. Torregrosa, *"Stability of a Fourth-Order Family of Iterative Methods for Solving Nonlinear Problems"*, Proceedings of the Ninth International Conference on Engineering Computational Technology, Naples, Italy, doi:10.4203/ccp.105.33.

Research Experience

2015–Present — **Graduate Research Assistant**, i-acoma group, University of Illinois Urbana-Champaign
Area: Computer Architecture
Topic: Application of extremely high frequency wireless on-chip communications in massive multi-core architectures
Advisor: Professor Josep Torrellas

2013–2015 — **Undergraduate Research Assistant**, Polytechnic University of Valencia
Area: Computational Mathematics
Topic: Design of high-order iterative methods for obtaining the roots of a nonlinear system of equations
Advisors: Professors Juan Ramón Torregrosa and Alicia Cordero

Research Interests

Computer architecture, network on chip, extremely high frequency wireless communications, multi-core and parallel architectures, programmability of parallel systems, computational mathematics

Awards, Honors and Scholarships

2017	**ISCA Travel Grant**
2015	**Award for the Second-Best Academic Record**, Class of 2015 Polytechnic University of Valencia
2015	**Undergraduate Thesis Distinction** Polytechnic University of Valencia
Fall 2014	**Erasmus Programme Grant** European Commission.
2013–2014	**Undergraduate Research Fellowship** Spanish Ministry of Education.
2011–2015	**4-Year Undergraduate Full Tuition Scholarship** Spanish Ministry of Education.

Skills

Languages	C/C++, Python, Java, Matlab, Shell/Bash scripting, Verilog, PHP, Javascript, MySQL
Frameworks	Flex, GNU Bison
Sim. Tools	Multi2Sim, MCPAT
Dev. Tools	Git, Vim
OS	Linux, Windows

Relevant Course Work

* indicates top of my class in the course

Graduate	Parallel Computer Architecture*, Computer System Organization, Operating System Design, Design and Implementation of Scripting Languages, Designing and Building Applications for Extreme Scale Systems, Wireless Networks and Mobile Systems.
Undergraduate	Microprocessors Based Systems*, Circuit Theory, Electronic Circuits and Devices*, Design of Telematic Services*, Information Management*, Communication Theory*, Probability and Random Signals*, Radiation and Wave Propagation, Optical and Digital Communications.

Selected Course Projects

Graduate	**CMat: The language and its interpreter** It implements an interpreter in Python for CMat; a blended subset of Matlab, C and Cool.
	Improving and characterizing low-layers for Wireless-Network-on-Chip A novel MAC (medium access control) protocol that adapts to the traffic characteristics of the network in real time. Also, a design and evaluation of a new mathematical model for the transmission channel in use for this architecture.
	AIA: A wireless-enabled chip multiprocessor An architecture with hybrid Network-on-Chip (wired+wireless). Targeting the reduction of latency for memory accesses that require several coherence messages.
Undergraduate	**Development of a VGA driver for an FPGA** Written in Verilog an implemented in an Altera DE2 Board (which included an Altera 90nm Cyclone II FPGA). The design software used was Altera Quartus II.
	Mastermind in 68000 assembly language with EASy68K Implementation of the classic Mastermind game in 68000 Assembly (the assembly language for the Motorola 68K-series microprocessors), to be later simulated with EASy68K.

Selected Personal Projects

(A more thorough list can be found on my personal website: afranques.com/projects)

2016–Present	**Quovis**. Android App for saving, organizing, and retrieving users' favorite locations.
Spring 2015	**Lazarius**. Android App for helping reduced-vision people move around cities in real time. Won second prize and Telefonica Award in the 2015 Spanish edition of Hack For Good.
Spring 2014	**2 Park**. Android App for managing parking spaces on the street in real time. Won Telefonica Award in the 2014 Spanish edition of Hack For Good.

Industry Experience

Summer 2010	**City Council of Montblanc**, Spain Systems and Network Administrator Intern Maintenance of Cisco devices, database management (SQL), and front-end web development (PHP, Javascript, CSS).

Teaching Experience

Fall 2016	**CS/ECE 439: Wireless Networks**, UIUC Teaching Assistant Occasional lecturer. Provided support and advice to 40+ students throughout development process of class projects.

Service

2013	**Incoming Exchange Students' Mentor** Polytechnic University of Valencia

Languages

English	Fluent
Spanish	Native
Catalan	Native